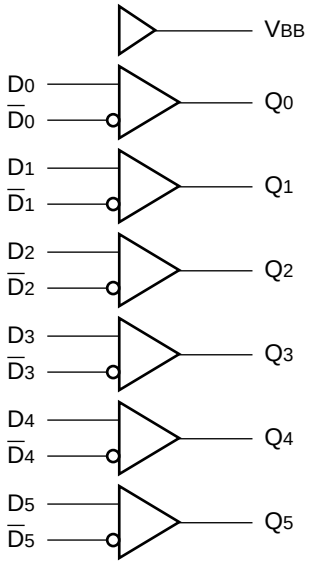
LOW-POWER HEX ECL-to-TTL TRANSLATOR

FEATURES

- **Max. propagation delay of 3.7ns**
- **I_{EE} min. of –37mA**
- **TTL outputs**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **25% faster than National's 325**
- **Differential inputs with built-in offset**
- **Voltage and temperature compensation for improved noise immunity**
- **V_{BB} output for single-ended use**
- **Internal 75KΩ input pull-down resistors**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

BLOCK DIAGRAM

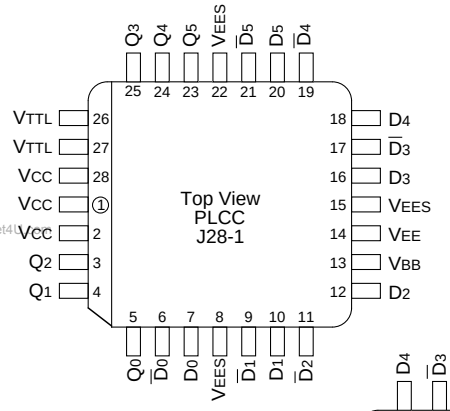


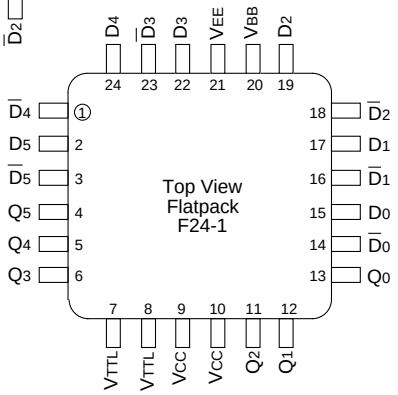
DESCRIPTION

The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides V_{BB} for single-ended operation or for use in Schmitt trigger applications. All inputs have 75KΩ pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The V_{TTL} and V_{EE} power may be applied in either order.

PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs
Q_0–Q_5	Data Outputs
V_{EES}	V_{EE} Substrate
V_{TTL}	TTL V_{CC} Power Supply
V_{CCA}	V_{CCO} for ECL Outputs

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Issue Date: July, 1999

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –4.8V unless otherwise specified, V_{CC} =V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	2.5	—	—	V	I_{OH} = –2.0mA	V_{IN} = V_{IH} (Max.)
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 24mA	V_{IN} = V_{IL} (Min.)
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible ±V_{CM} with Respect to V_{BB}	
I_{IH}	Input HIGH Current	—	—	350	µA	V_{IN} = V_{IH} (Max.), D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = V_{IL} (Min.)	
I_{IL}	Input LOW Current	0.5	—	—	µA	V_{IN} = V_{IH} (Min.), D_0–D_5 = V_{BB}	
I_{OS}	Output Short Circuit Current	–150	–80	–60	mA	V_{OUT} = GND	
I_{EE}	V_{EE} Power Supply Current	–37	–24	–17	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current	—	42	65	mA	D_0–D_5 = V_{BB}	
V_{BB}	Ouptut Reference Voltage	–1380	–1320	–1260	mV	I_{VBB} = –2.1mA	
V_{IH}	Single-Ended Input HIGH Voltage	–1165	—	–880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	–1810	—	–1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to V_{BB})	

AC ELECTRICAL CHARACTERISTICS

PLCC/FLATPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	2100	2900	ps	C_L = 15pF, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	3100	3700	ps	C_L = 50pF, Figure 2

SWITCHING WAVEFORM

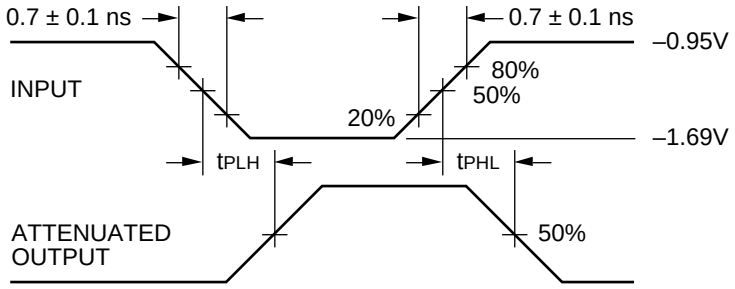


Figure 1. Propagation Delay

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

TEST CIRCUITS

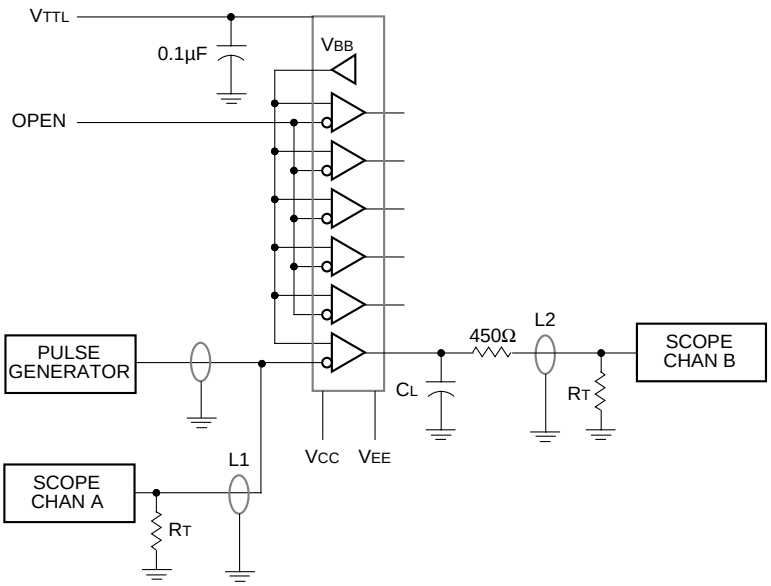


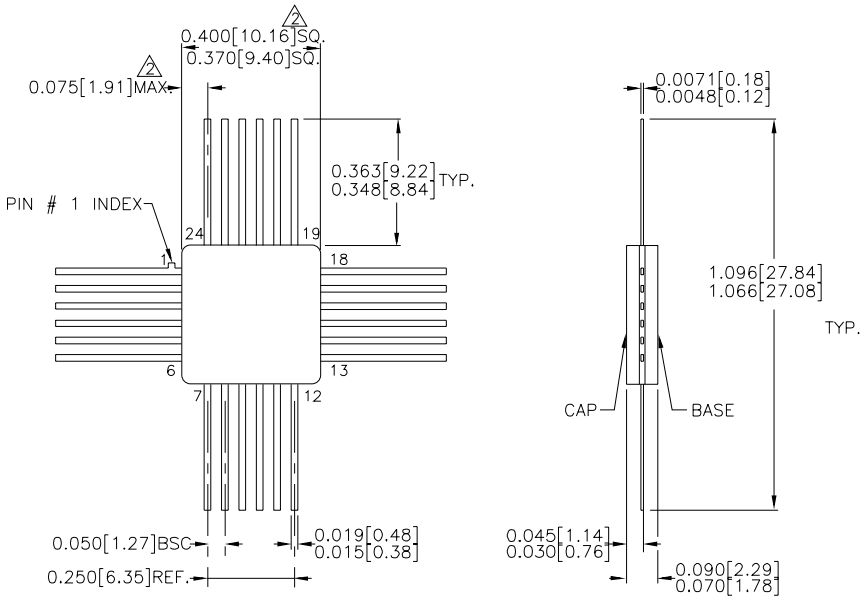
Figure 2. AC Test Circuit for 15pF Loading

NOTES:
V_{CC} = 0V, V_{EE} = –4.5V, V_{TTL} = +5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1µF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 500Ω to GND
C_L = Fixture and stray capacitance = 3pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S325FC	F24-1	Commercial
SY100S325JC	J28-1	Commercial
SY100S325JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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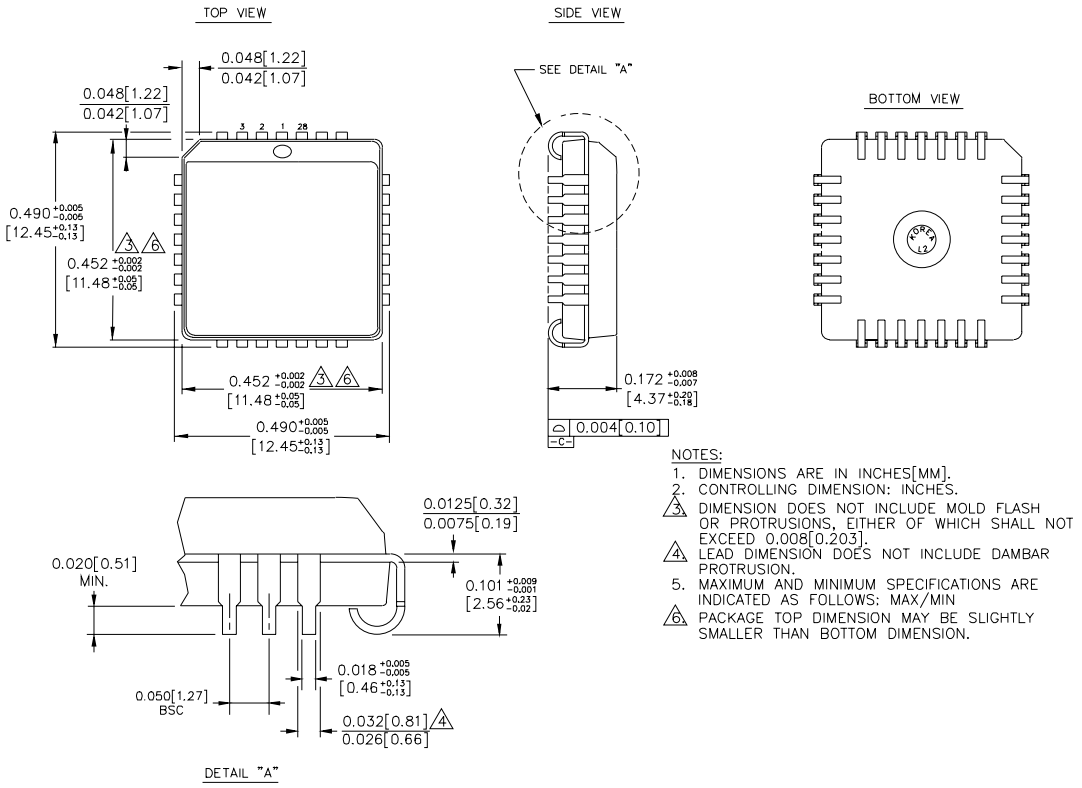
28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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